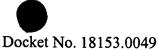
CLAIMS:

What is claimed is:

- 1 1. A method of multiplying two maximally negative fractional numbers to produce a
- 2 32-bit result, comprising:
- 3 fetching operands from a source location:
- 4 performing a multiplication operation on the operands; and
- detecting that a result output of the multiplication operation corresponds to a 5
- maximally negative result; 6
- 7 wherein the maximally negative result indicates that the operands are two
- maximally negative fractional numbers. 8
- 2. The method according to claim 1, further comprising the step of correcting the 1
- 2 result output to produce a maximally positive result output.
- 1. 3. The method according to claim 2, wherein the step of detecting that the result
- output of the multiplication operation corresponds to a maximally negative result includes 2
- the step of examining bits in a set of bits representing the result output. 3
- The method according to claim 3, wherein the step of detecting that the result 4. 1
- output of the multiplication operation corresponds to a maximally negative result includes 2
- the step of determining that the bits in the set of bits representing the result have a 3
- particular bit combination. 4



- 5. The method according to claim 4, wherein the bits in the set of bits are the thirtieth 1
- and thirty-first bits in the set of bits representing the result output. 2
- The method according to claim 4, wherein the particular bit combination for the 1 6.
- bits in the set of bits representing the result output is one and zero respectively. 2
- 7. The method according to claim 2, wherein the step of correcting the result to 1
- produce a maximally positive result includes the step of generating a control signal. 2
- The method according to claim 7, wherein the step of correcting the result to 8. 1
- produce a maximally positive result includes the step of modifying a negate control signal 2
- 3 based on the control signal.
- The method according to claim 8, wherein the step of correcting the result to 9. 1
- produce a maximally positive result includes the step of performing a two's compliment on 2
- 3 the result output.
- The method according to claim 9, further comprising: 1 10.
- accumulating the maximally positive result output to an accumulator. 2
- 1 11. The method according to claim 1, further comprising the step of fractionally
- 2 aligning the result output.



- 12. The method according to claim 11, wherein the step of fractionally aligning the 1
- result output includes the step of shifting a set of bits representing the result output to the 2
- left by one bit to discard the most significant bit of the set of bits representing the result 3
- output and insert a zero as the least significant bit of the set of bits representing the result 4
- 5 output.
- 13. The method according to claim 1, further comprising the step of sign extending the 1
- 2 output result.
- 1 14. The method according to claim 13, wherein the result output is extended from a 32-
- 2 bit result to a 40-bit result.
- 15. A processor for multiplication operation instruction processing, comprising: 1
- 2 a DSP unit operable to:
- 3 fetch operands from a source location;
- 4 perform a multiplication operation on the operands; and
- a control block operable to detect that a result output of the multiplication operation 5
- 6 corresponds to a maximally negative result;
- wherein the maximally negative result indicates that the operands are two 7
- 8 maximally negative fractional numbers.
- The processor according to claim 15, further comprising a negate logic operable to 1 16.
- correct the result output to produce a maximally positive result output. 2



- 1 17. The processor according to claim 16, wherein the control block detects a maximally
- 2 negative result by examining bits in a set of bits representing the result output.
- 1 18. The processor according to claim 17, wherein the examination of the bits in the set
- 2 of bits is to determine a particular bit combination.
- 19. 1 The processor according to claim 18, wherein the bits in the set of bits are the
- thirtieth and thirty-first bits in the set of bits representing the result output. 2
- 1 20. The processor according to claim 18, wherein the particular bit combination for the
- bits in the set of bits representing the result output is one and zero respectively. 2
- 1 21. The processor according to claim 16, wherein the control block generates a control
- 2 signal.
- 1 22. The processor according to claim 21, wherein the control signal is operable to
- 2 modify a negate control signal.
- 1 23. The processor according to claim 22, wherein the negate logic is operable to
- perform a two's compliment operation on the result output based on the negate control 2
- 3 signal.

- 1 24. The processor according to claim 23, further comprising:
- An accumulator operable to accumulate the maximally positive result output.
 - 1 25. The processor according to claim 15, further comprising fractionally aligning logic
 - 2 operable to fractionally align the result output.
 - 1 26. The processor according to claim 25, wherein the fractionally alignment logic shifts
 - a set of bits representing the result output to the left by one bit to discard the most
 - 3 significant bit of the set of bits representing the result output and insert a zero as the least
 - 4 significant bit of the set of bits representing the result output.
 - 1 27. The processor according to claim 15, further comprising sign extension logic
 - 2 operable to sign extend the result output.
 - 1 28. The processor according to claim 27, wherein the sign extension logic extends the
 - 2 result output from a 32-bit result to a 40-bit result.